# F-INDUCTOR AND BC-MOS TECHNOLOGY FOR MONOLITHIC SILICON RF IC's

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## ABSTRACT

A high performance spiral inductor and a RF-optimized MOSFET are developed for monolithic silicon RF application. The new inductor is made on the standard CMOS processed wafer using flip-chip bonding technology. Its floating-in-air structure enables to achieve more than 18GHz resonant frequency at 4.8nH inductance, as well as the good Q-factor. The RF-optimized MOSFET adopts the buried channel and the profiled junction structure for larger Gm and smaller $C_{GD}$. The measurement results show the improvement of Gm by 30% and $f_T$ by 45%, and the decrease of $C_{GD}$ by 52%, compared with that of the conventional MOSFET.

## INTRODUCTION

The increasing demand for low cost and one-chip integration with CMOS digital circuit has driven a Si-MOSFET technology into RF application field. In the view of the mature technology, however, the high-Q inductor on the lossy silicon substrate and the high-performance MOSFET without pushing channel length to scale down are still in under developed level. To get a good inductor, there have been several efforts such as the use of the high resistivity wafers[1], the suspended inductor[2] and the inductor on thick insulator[3], but neither get the low cost nor the compatibility with the process of the standard digital IC's. Also to improve RF performance of MOSFET, there have been some approaches which are the reduction of the channel length[4] and the optimization of layout[5], but their DC optimized structure could not obtain the best RF performances.

In this paper, we present two technologies for monolithic silicon RF circuit; Floating-in-air inductor (F-inductor) and Buried Channel MOSFET with profiled junction (BC-MOS). F-inductor is a monolithic inductor on silicon substrate, which exists on the top of the longer than 10μm bumps above the area of the active devices or the digital circuitry. Its air gap between the inductor track metal and the substrate can reduce parasitic capacitance so that higher resonant frequency and higher Q can be obtained. BC-MOS is a RF-optimized MOSFET which adopts the buried channel for the larger transconductance, Gm, and the profiled source/drain junction for the lower gate to drain capacitance, $C_{GD}$. The measured results show that F-inductor has higher resonant frequency than the spiral inductor in GaAs and BC-MOS has higher cutoff frequency, $f_T$, than the conventional surface channel MOSFET.

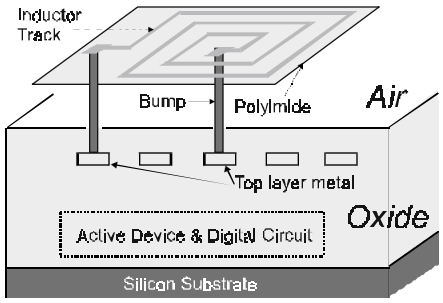


Fig.1. Schematic view of F-inductor

## FLOATING-IN-AIR INDUCTOR (F-INDUCTOR) TECHNOLOGY

Figure 1 shows the schematic view of the F-inductor structure. F-inductor exists in air, and is connected to top layer metal of standard CMOS circuit through long bumps, which act as an electrical connector and a mechanical supporter for the inductor track metal. Due to the enough height, F-inductor can be integrated over the area of the other circuit components without coupling effects.

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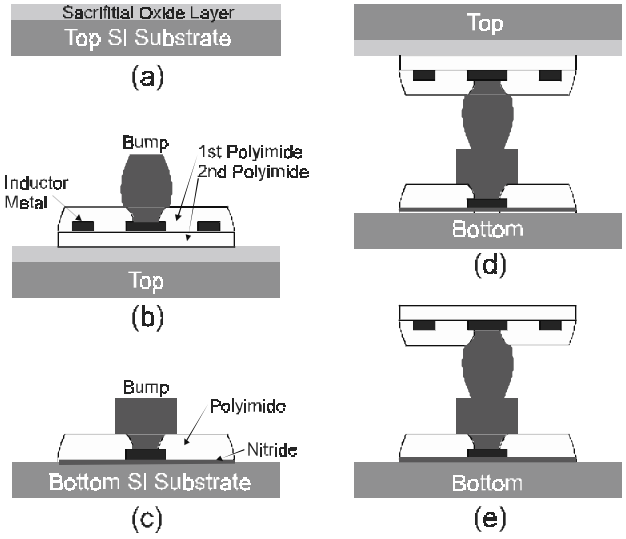


Fig.2. Process sequence; (a) Sacrificial oxide deposition, (b) Inductor formation, (c) Signal line formation, (d) Attach the inductor on signal line, (e) Detach the inductor.

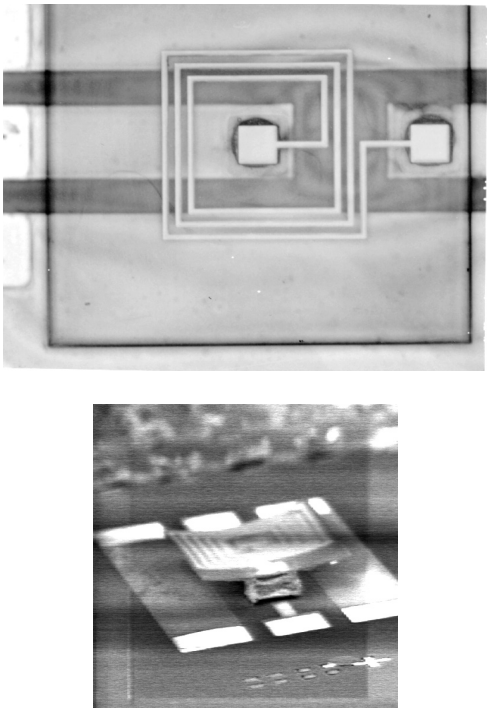

Fig.3. Photomicroscopy and SEM view of the fabricated F-inductor

The fabrication of F-inductor is as follows. Inductor track metal is made on the dummy or top substrate such as silicon or glass. It is, then, attached to the signal line of a CMOS processed wafer with flip-chip bonding technology. The top substrate is detached to remain inductor on signal lines. Its detail fabrication sequence is shown in Fig. 2. The sacrificial oxide which will be etched at detaching of the inductor, is deposited on top silicon substrate. Au/Al/Ni for the inductor track metal are deposited and patterned between the deposition processes of two polyimide layers, where Au is the main inductor metal. After the patterning the bump pads, Indium is grown and lifted off to make the bumps on the pads. These bumps are attached to the bumps fabricated on the metal signal lines of the bottom silicon substrate with flip-chip bonding machine. These attached inductors are dipped in the oxide etching solution to remove the sacrificial oxide layer. After the etching, the top silicon substrate is detached automatically to make F-inductor with the developed detaching method. Figure 3 shows the fabricated 3-turn F-inductor of which inductor metal has 0.7um thickness, 10um width and 10um space with 18um height bumps.

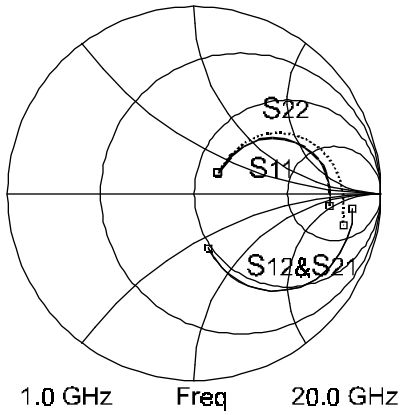


Fig.4. Deembedded S-parameters of F-inductor

The frequency dependent S-parameters of F-inductor are measured with on-wafer measurement to 26.5GHz and the pad parasitic is deembedded with dummy patterns. Figure 4 shows the measured s-parameters of 5-turn inductor. The resonant frequency is compared with that of spiral inductor on GaAs substrate as shown in Fig. 5. The measured resonant frequency of F-inductor is larger than 18GHz of which value is higher than that of the spiral inductor on GaAs. Quality factor is shown in Fig.6. Q is decreased as the increase of the inductance, and those values are higher than the

reported data with the same metal thickness[3]. The reason of the higher resonant frequency and Q is the smaller parasitic capacitance of F-inductor. The modeling for F-inductor with the conventional π-equivalent circuit using HP-MDS shows the small parasitic capacitance to be less than 18fF as shown in Fig.7.

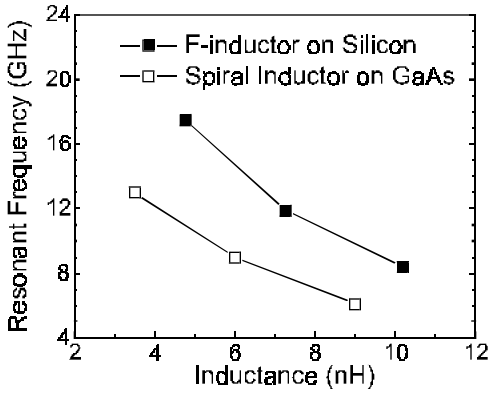


Fig.5. Comparison of Resonant Frequency

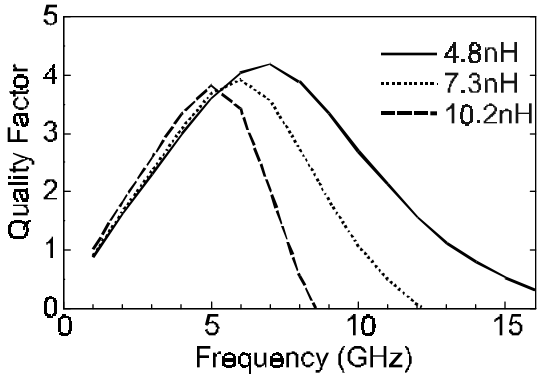


Fig.6. Quality Factor as the variance of frequency

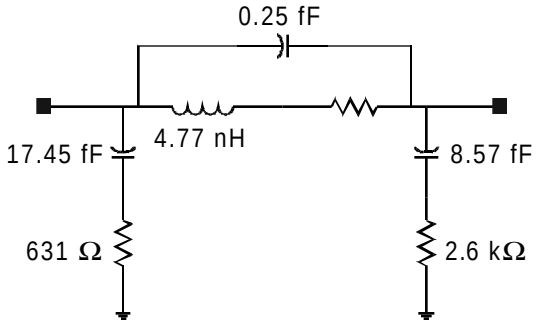


Fig.7. π-equivalent circuit model

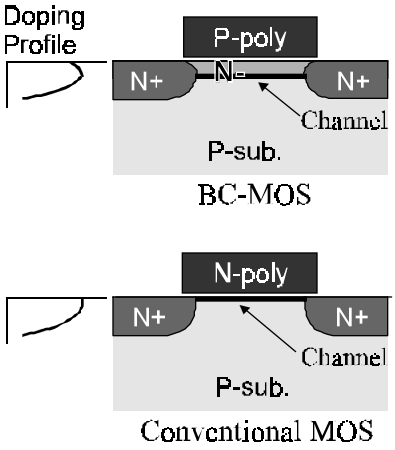


Fig.8. BC-MOS and the conventional MOS structure

## BURIED CHANNEL MOSFET WITH PROFILED JUNCTION (BC-MOS)

The structure of BC-MOS consists of the buried channel structure and the profiled source/drain junction as shown in Fig. 8. The purpose of the buried channel is to use the mobility characteristic which is higher in bulk than in surface. Its structure has the shallow n-type region which is initially depleted by p-type polysilicon gate and p-type silicon substrate. When the positive gate bias is applied, a channel is generated in bulk through the reduction of the depletion region of the shallow n-type region, compared with the surface channel generation in the conventional MOSFET. With the help of the higher mobility of the buried channel, BC-MOS can obtain a much larger Gm at low gate bias condition. The profiled source/drain junction is to reduce the parasitic gate to drain capacitance, $C_{GD}$ by the reduction of the surface doping density of the junction and the gate overlap over the junction. The device performance is not degraded because of the enough junction overlap and the doping density at the buried channel depth, even though gate overlap at surface decreases.

Figure 9 shows DC measured data of BC-MOS compared with that of the conventional surface MOSFET. In threshold voltage, $V_{TH}$, both BC-MOS and the conventional MOSFET have similar values as shown in the inset, but in Gm, BC-MOS has large value of 220mS/mm compared with 170mS/mm of conventional MOSFET. Also $C_{GD}$ is measured to be

28 fF, only being 52 % of the conventional junction. The $f_T$, extracted from the |H21|, is 13.68 GHz which is larger by 45 % than 9.45 GHz of the conventional MOSFET at 1.5V gate bias as shown in Fig. 10. The $f_T$ curve as a function of gate bias shows that the difference in $f_T$ from BC-MOS to the conventional MOSFET is large at lower gate bias and decreases as the bias increases. This tendency is caused by the fact that the buried channel goes upward to surface to degrade the mobility as the gate bias increases. The large Gm in low gate bias enables BC-MOS to be more applicable to the low power circuits. In addition, BC-MOS has smaller variation of $f_T$ than the surface channel MOSFET, which means that it has better performance in low noise amplifier and has less dependence on the gate biasing conditions

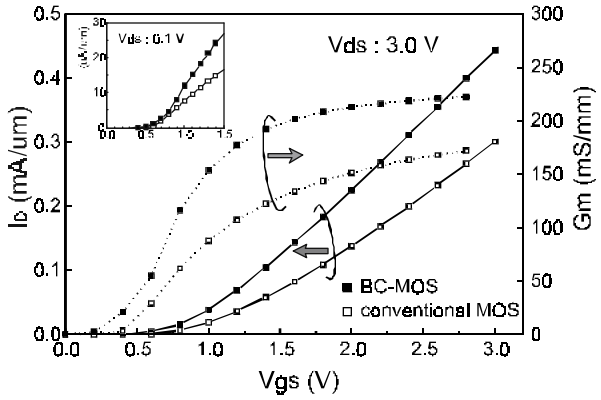


Fig.9. Ids-Vgs curve of BC-MOS compared with that of the conventional MOS.

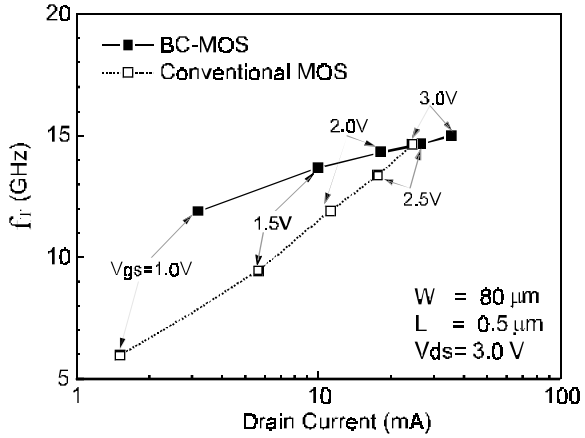


Fig.10. $f_T$ as a fuction of gate bias and drain current.

## CONCLUSION

A CMOS-compatible F-inductor and a RF-optimized BC-MOS have been developed to provide a low cost, high RF-performance technology for monolithic Si RF-system. Using new technologies, the fabricated F-inductor has more than 18GHz of resonant frequency, being higher than that in GaAs, and BC-MOS has 13.68GHz of $f_T$, improving 45 % of the conventional MOSFET. These results shows that F-inductor and BC-MOS technology for the passive and the active device are applicable to several GHz Silicon RF systems.

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